What is claimed is:

1. A semiconductor memory device comprising:

an array of memory cells;

an address input circuit for receiving an external address in response to an address clock signal;

a selecting circuit for selecting a memory cell in response to an address output from the address input circuit;

a data output circuit for outputting data read out from the selected memory cell in response to first and second data clock signals; and

an internal clock generating circuit for generating the address clock signal and the first and second data clock signals in response to an external clock signal and complementary clock signal, wherein the address clock signal and the first and second data clock signals have twice the frequency of the external clock signal in a test mode.

2. The semiconductor memory device of claim 1, wherein the internal clock generating circuit generates the address clock signal and the first and second data clock signals having the same frequency as the external clock signal in a normal mode.

3. The semiconductor memory device of claim 1, further comprising:

a data input circuit for receiving external data in response to the first and second data clock signals;

a write driver circuit for writing data from the data input circuit to the selected memory cell of the array of memory cells; and

a read out circuit for reading out data from the selected memory cell and sending it to the data output circuit.

4. The semiconductor memory device of claim 1, wherein the internal clock generating circuit comprises a synchronous mirror delay circuit.

5. The semiconductor memory device of claim 1, wherein the semiconductor memory device is a double data rate (DDR) memory device.

6. The semiconductor memory device of claim 1, wherein, in the test mode, the internal clock generating circuit generates the address clock signal at every 1/4 period of the external clock signal, the first data clock signal at every 0 and 1/2 periods of the external clock signal, and the second data clock signal at every 1/4 and 3/4 periods of the external clock signal.

7. The semiconductor memory device of claim 1, wherein, in a normal mode, the internal clock generating circuit generates the address clock signal at every 0 period of the external clock signal, the first data clock signal at every 0 period of the external clock signal, and the second data clock signal at every 1/2 period of the external clock signal.

8. A semiconductor memory device comprising:

an array of memory cells;

an address input circuit for receiving an external address in response to an address clock signal;

a selecting circuit for selecting a memory cell in response to an address output from the address input circuit;

a data output circuit for outputting data read out from the selected memory cell in response to first and second data clock signals;

a first clock generating circuit comprising a first synchronous mirror delay circuit, for generating a first internal clock signal and a second internal clock signal having 0T and T/4 phases of an external clock signal, respectively, where T is a period of the external clock signal; and

a second clock generating circuit comprising a second synchronous mirror delay circuit, for generating a third internal clock signal and a fourth internal clock signal having a T/2 and 3T/4 phases of the external clock signal, respectively;

wherein, in a test mode, the address clock signal is generated in synchronization with the first, second, third and fourth internal clock signals, the first data clock signal is generated in synchronization with the first, second and third internal clock signals, and the second data clock signal is generated in synchronization with the second and fourth internal clock signals.

9. The semiconductor memory device of claim 8, further comprising:

a first decoding circuit for decoding the first and second internal clock signals in response to control signals and outputting first, second and third decoding signals;

a second decoding circuit for decoding the first and second internal clock signals in response to the control signals and outputting fourth, fifth and sixth decoding signals; and

a third clock generating circuit for generating the first and second data clock signals and the address clock signal in response to the first, second, third, fourth, fifth and sixth decoding signals.

10. The semiconductor memory device of claim 8, wherein, in a normal mode, the address clock signal is generated in synchronization with the first internal clock signal, the first data clock signal is generated in synchronization with one of the first and second internal clock signals, and the second data clock signal is generated in synchronization with one of the third and fourth internal clock signals.

11. The semiconductor memory device of claim 8, further comprising:

a data input circuit for receiving external data in response to the first and second data clock signals;

a write driver circuit for writing data from the data input circuit to the selected memory cell of the array of memory cells; and

a read out circuit for reading out data from the selected memory cell and sending it to the data output circuit.

12. The semiconductor memory device of claim 8, wherein the semiconductor memory device is a double data rate (DDR) memory device.

13. The semiconductor memory device of claim 8, wherein the first synchronous mirror delay circuit comprises:

a first clock buffer for generating a first reference clock signal in response to the external clock signal;

a first delay monitor circuit for delaying the first reference clock signal;

a first forward delay array for sequentially delaying an output clock signal of the first delay monitor circuit in a forward direction to generate first delay clock signals;

a first mirror control circuit for receiving the first delay clock signals and the first reference clock signal and detecting one of the first delay clock signals synchronized with the first reference clock signal;

a first backward delay array for delaying the detected delay clock signal in a backward direction to output the first internal clock signal;

a first unit delay element for delaying the first internal clock signal by a delay time of T/8;

a second forward delay array for sequentially delaying the first internal clock signal in a forward direction to generate second delay clock signals;

a second mirror control circuit for detecting one of the second delay clock signals synchronized with the output clock signal of the first unit delay element; and

a second backward delay array for delaying the detected delay clock signal in a backward direction to output the second internal clock signal.

14. The semiconductor memory device of claim 8, wherein the second synchronous mirror delay circuit comprises:

a second clock buffer for generating a second reference clock signal in response to an external clock signal;

a second delay monitor circuit for delaying the second reference clock signal;

a third forward delay array for sequentially delaying an output clock signal of the second delay monitor circuit in a forward direction to generate third delay clock signals;

a third mirror control circuit for receiving the third delay clock signals and the second reference clock signal and detecting one of the third delay clock signals synchronized with the second reference clock signal;

a third backward delay array for delaying the detected delay clock signal in a backward direction to output the third internal clock signal;

a second unit delay element for delaying the second internal clock signal by a delay time of T/8;

a fourth forward delay array for sequentially delaying the third internal clock signal in a forward direction to generate fourth delay clock signals;

a fourth mirror control circuit for detecting one of the fourth delay clock signals synchronized with the output clock signal of the second unit delay element; and

a fourth backward delay array for delaying the detected delay clock signal in a backward direction to output the fourth internal clock signal.

15. A semiconductor memory device, comprising:

a memory cell array for storing data, wherein the memory cell array comprises a plurality of memory cells;

an address input circuit for receiving external address signals in synchronization with an address clock signal output from an internal clock generating circuit;

a decoder for decoding addresses output from the address input circuit and selecting a memory cell that is associated with the addresses output from the address input circuit of the memory cell array;

a data input circuit for receiving a first and second data clock signal from an internal clock generating circuit;

a data output circuit for outputting data from the selected memory cells; and

an internal clock generating circuit for receiving external clock signals and generating the address clock signal and the first and second data clock signals, wherein the address clock

signal and first and second data clock signals have twice the frequency of the external clock signals according to a mode of operation.

16. The semiconductor memory device of claim 15, further comprising:

a write driver circuit for writing data received from the data input circuit to the selected memory cell from the array of memory cells; and

a read-out circuit for reading out data from the selected memory cell from the array of memory cells.

17. The semiconductor memory device of claim 15, wherein the internal clock generating circuit generates the address clock signal and the first and second data clock signals having the same frequency as the external clock signal in a normal mode.

18. The semiconductor memory device of claim 15, wherein, in the test mode, the internal clock generating circuit generates the address clock signal at a 1/4 period of the external clock signal, the first data clock signal at a 0 and 1/2 periods of the external clock signal, and the second data clock signal at a 1/4 and 3/4 periods of the external clock signal.

19. The semiconductor memory device of claim 15, wherein, in a normal mode, the internal clock generating circuit generates the address clock signal at a 0 period of the external clock signal, the first data clock signal at a 0 period of the external clock signal, and the second data clock signal at a 1/2 period of the external clock signal.